High density PCB technology for high reliability applications using Low CTE material

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Abstract
The space- and other high reliability markets are continuously driven towards an increased use of deeply integrated electronics. The increasing demand for complexity and functionality results in the use of large package components with a high number of I/Os. In order to allow the use of components with high pin counts up to 1752, complex high-density interconnect (HDI) printed circuit board (PCB) technology is required. Reconciling the use of multiple laser-drilled microvia levels in a stacked configuration with the reliability requirements for space is challenging when using heritage dielectric materials. The use of ceramic filled low CTE material allows the manufacturing of complex HDI PCB technology with a high reliability.

The work presented in this paper is part of an ongoing European (Horizon 2020) "COMAP-4S" project on components and macro components packaging for space. The Project is coordinated by SAFRAN ELECTRONICS AND DEFENSE with partners ACB, TUB and NANOXPLORE. The most complex PCB technology targeted within the project is four levels of microvias, requiring the use of low CTE laminate material. The reliability of different microvia configurations from all four levels staggered to all stacked was evaluated using test methods as described in ESA's ECSS-Q-ST-70-60C standard for qualification and procurement of printed circuit boards. The test results of various material-level reliability tests, interconnection stress testing (IST) and reflow simulation combined with rework and traditional thermal cycling are provided to demonstrate a high reliability of the different via configurations and overall PCB technology.

Introduction
Microvia technology has been used in the industry for multiple decades. Overall, this technology is considered reliable when manufactured properly. High reliability markets give preference to copper-filled microvias as they have a higher reliability compared to resin-filled microvias. The use of copper-filled microvias also allows the use of stacked microvia technology.
Today's drivers and technology parameters for HDI PCB technology in space projects, limit the PCB complexity to a maximum of three levels of microvias [1]. This three level microvia configuration is limited to semi-stacked technology where two levels of stacked microvias are staggered with the third level. Stacking three levels of microvias is considered a reliability risk.
One of the goals of the COMAP-4S project is to consolidate HDI PCB technology beyond this level of complexity.

One of the key aspects to achieve a reliable four level microvia technology is the material choice. For space and other high reliability applications, polyimide remains the material of preference. Polyimide has a high Tg around 250°C but also a relatively high coefficient of thermal expansion (CTE). Typical datasheet values for the CTE of polyimide are 50 ppm/°C below Tg and 150 ppm/°C above Tg. Measured CTE values for polyimide HDI constructions are easily another 10ppm/°C larger. These higher CTE values are explained by the use of thin glass weave prepreg plies in typical HDI constructions [2]. The use of low CTE material instead of polyimide has two main advantages. The mismatch between the CTE of the component and the PCB material may result in reliability issues on component or component connection level. Using low CTE material on PCB level will lower the mismatch and lead to a more reliable PCBA. Secondly, the use of low CTE material has a positive impact on reducing failure mechanisms on PCB level. Interconnection failures on HDI PCBs may occur in microvias, buried vias and plated through holes. Using materials with a lower CTE, results in less expansion during assembly and during mission, and reduces the risk of typical fatigue failures like barrel cracks. For microvias specifically, separation of the microvia from the target pad is a possible failure mechanism. In 2018, IPC released a white paper warning the industry about this weak microvia interface issues [3]. The verification of microvia quality and reliability was therefore chosen as focus within this project.

When discussing microvia reliability, the laser drill diameter is an important parameter. Typical aspect ratios should be below 1 to allow a proper laser drill quality and a qualitative plating of the via. Various test campaigns show that using larger laser drill diameters result in a more reliable microvia [4]. Typical laser drill diameters used for space applications are 150um and 175um. Within this project 125um and 150um laser drill diameters were used and reliability was compared. Since a single ply configuration was used for the microvia layers, aspect ratios were well below one. Further details about the microvia configuration are described in the next section.

Test Vehicle description

The PCB test vehicle panels used within this project contain the following features.

- PCB TV with different microvia daisy chain patterns
- A/B coupon with PTHs
- B coupons with 4 levels of microvias and buried vias.
- E coupons for intralayer insulation resistance and dielectric withstanding voltage
- H coupons for interlayer insulation resistance and dielectric withstanding voltage
- P coupons for Peelstrength testing
- K coupons for thermal analysis
- IST coupons of which one type of TVX and six types of SLX coupons

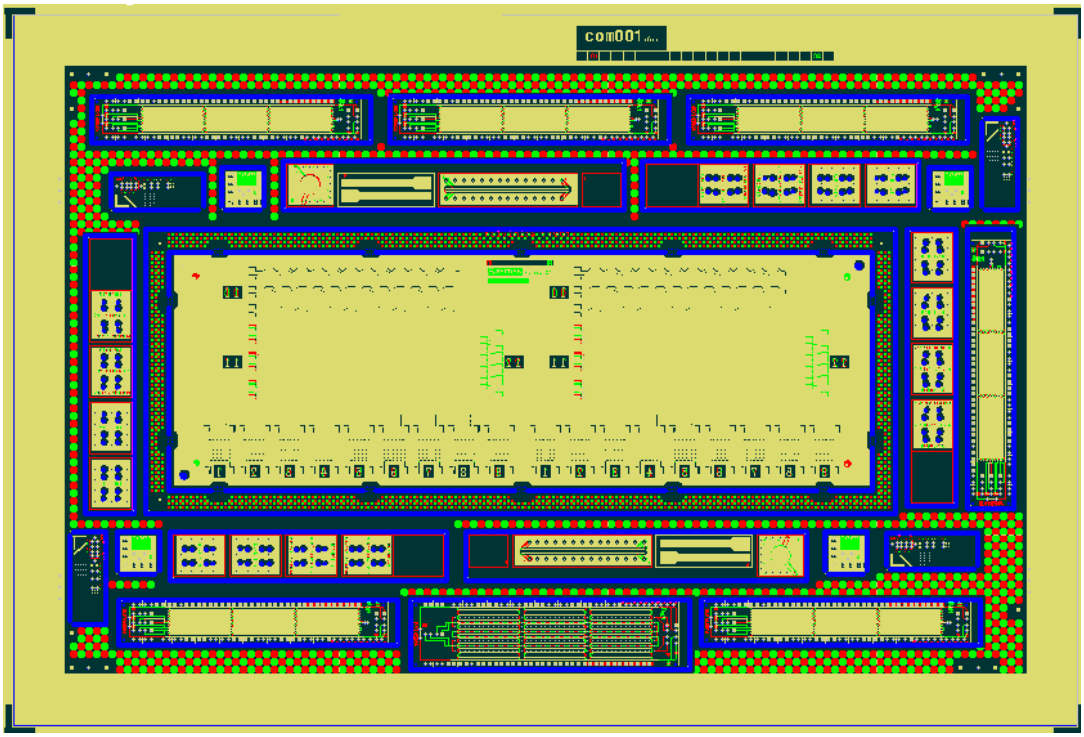


Figure 1. PCB production panel with central PCB TV and various coupons for reliability testing.

The HDI PCB technology used contains four levels of microvias. In total three different configurations and two different laser drill diameters are tested. In all configurations every microvia level was copper filled. The first variable is the laser drill diameter. With diameters of 150um and 125um, two sizes of laser drill diameter are benchmarked. The second level of variables is in the microvia configuration. Three different configurations are used in the test campaign. The all-staggered configuration is considered as the most reliable but is not considered as a good solution on design level as the staggered configuration reduces the routing space significantly. The intermediate solution in which the top level of microvias is staggered with the three lower levels of stacked microvias was chosen as a solution that allow much more design freedom. The full stacked configuration is considered the worst case with respect to reliability but best case when taking design freedom into account. The as deigned microvia annular ring for capture and target layers was chosen as 87.5um for 125um and 100um for the 150um laser drilled vias. This corresponds to 300 and 350um pad size respectively. The buried vias are 350um in drill diameter and pad size was set at 630um to allow a 140um as designed annular ring. The pitch between laser drill diameter of the fourth level and buried via is 400um as designed. No microvias on all levels were positioned above the buried vias.

The dielectric material used within the frame of this project is a ceramic filled low CTE material. The prepreg definition between microvia layers is a single ply configuration with a nominal thickness around 80um. This thin prepreg configuration allows the drilling of smaller laser drill diameters. An important remark needs to be made when using low CTE material. Since the presence of ceramics in the resin system reduces the flow behavior of the resin significantly, thick copper and prepreg resin filling of vias is to be avoided. For this reason, the buried vias are plugged with a plugging paste prior to the microvia laminations. Soldermask was used in combination with ENEPIG as surface finish. The below table 1 shows the technology overview and figure 2 shows the build-up and different via configurations.

Table 1. Technology parameters for HDI low CTE technology

Technology Parameter	Feature value
Dielectric Material	Ceramic filled Low CTE material (Tg: >250°C, CTE-z: 15-25 ppm/°C < Tg)
Number of layers	14 layers
Number of laminations	5 laminations
number of microvia levels	4 levels
µ-via configurations	full stacked, semi stacked, full staggered
Thickness	1.7mm
conductor width and spacing plated layers (12um+plating)	50/50um , 65/65um , 75/75um
conductor width and spacing innerlayers (17um)	50/50um , 65/65um , 75/75um
Filling for core vias	Via plugging (without cap plating)
Nonfunctional pads	present on all layers
Plated through hole diameter	400um
Plated through hole pad size	700um
Buried via diameter	350um
Buried via pad size	630um
µ-via diameter	125um , 150um
µ-via pad size	300um , 350um
Surface finish and solder mask	ENEPIG with soldermask

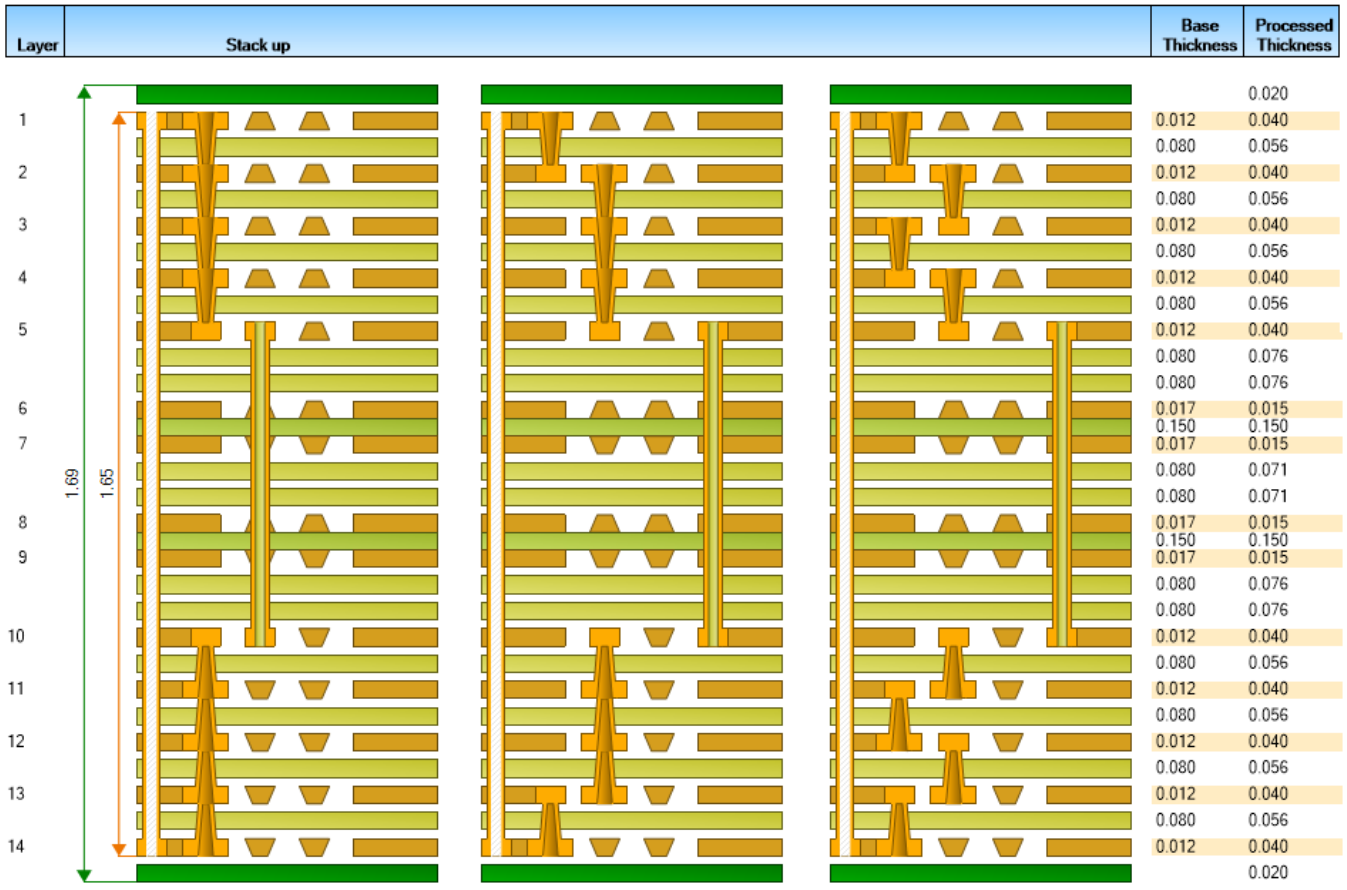


Figure 2. Build-up overview with 3 different microvia configurations.

Experimental Methodology

The reliability tests performed in the frame of the European COMAP-4S project are mainly focusing on ESA requirements as described in the ECSS-Q-ST-70-60C standard for qualification and procurement of printed circuit boards [5]. In this paper the methodology and results of thermal analyses, thermal stress testing (Group 3), IST testing and assembly and life testing (Group 4) are discussed in detail.

Thermal Analyses Test

It is important to have an actual idea of the CTE of the used HDI build-up. As explained above, the CTE can be significantly higher compared to technical datasheet values. The reason for this is because typical CTE test vehicles are made out of thick double-sided constructions that usually tend to have a low resin content.

Coupons used for the thermal analyses test were free of copper on each layer. The Thermal Mechanical Analyses (TMA) method as described in method 2.4.24 IPC-TM-650 was used to determine the glass transition temperature (Tg) and CTE in the z-axis of the HDI buildup.

Thermal Stress Test

As defined in § 9.5 of the ECSS-Q-ST-70-60C, there are two thermal stress methods applied to verify the internal structural integrity of the PCB on A/B coupons. The solder bath float, in conformance with condition A of the test method 2.6.8.e of IPC-TM-650, is applied 3 times during 10 seconds at a solder bath temperature of 288°C. The second thermal stress test is the rework simulation. This is performed in conformance to paragraph §9.5.4 of the ECSS-Q-ST-70-60C. this test is performed by manual soldering a wire on one of the vias or µ-via pads of the A/B coupons for a total of 11 heating cycles. The sections are inspected with a microscope at magnifications ranging from x50 to x1000. The brightfield mode of the microscope is used to analyse the metallization quality. The darkfield mode provides the best contrast to analyse the quality of dielectric material. Acceptance criteria of the sections were verified in conformance to the table under §10.2 of the ECSS-Q-ST-70-60C.

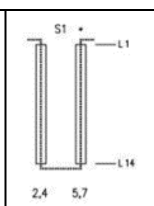
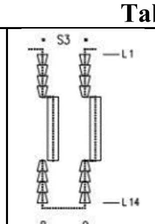
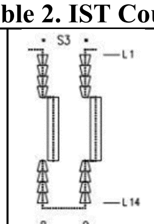
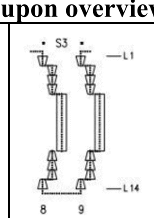
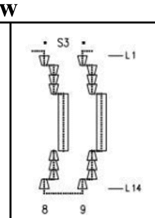
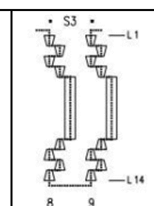
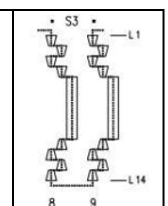
Interconnection stress testing (IST)

IST is an important test that is used within the ECSS-Q-ST-70-60C to evaluate via reliability on both procurement and process control level. It is a current induced thermal cycling test and is described in IPC-TM-650 2.26A (Method A). the tested uses specific daisy chain coupon designs that represent the PCB design features and different via configurations. For HDI technology PTH coupons and coupons combining microvias and buried vias are tested. The coupons are heated using a power circuit and the resistance is constantly monitored using the sense circuit(s).

IST coupons are first subjected to a total of six preconditioning cycles at 230°C which should represent a worst case SnPb assembly process with subsequent repair and rework operations. The plated through holes and buried via sequences are cycled from room temperature to 150°C in a 3-minute heating and 2 minute cooling cycle. Subsequently, a total of 500 cycles are applied and acceptance criteria is that the resistance increase should not exceed 5% before 400 cycles. The cycles to assess the microvia reliability are performed after initial 500 cycles for the buried via reliability assessment. Microvia testing is performed at a different temperature as microvias typically experience lower stress during cycling. The cycling temperature of microvias is 190°C and the resistance increase threshold is set at 4% after 400 cycles.

To compare the multiple microvia configurations from full staggered to fully stacked and with two different microvia diameters, multiple IST coupon designs were needed. Table 2 gives the overview of the seven different IST coupon types with via drill diameters.

Table 2. IST Coupon overview

Via Structure							
IST coupon ref.	TVX14236A	SLX14256A	SLX14257A	SLX14258A	SLX14259A	SLX14260A	SLX14261A
PTH Ø	400um	NA	NA	NA	NA	NA	NA
µ-via Ø	NA	125um	150um	125um	150um	125um	150um
Buried via Ø	NA	350um	350um	350um	350um	350um	350um

Assembly and life test (Group 4)
To assess the via reliability and verify the structural integrity of the HDI PCB technology after assembly and lifetime, a group 4 test as described in paragraph §9.6.2 of the ECSS-Q-ST-70-60C has been carried out.
This test flow contains on PCB verification level:

- Pre-conditioning/ baking of the PCB and test coupons at 120°C for 8 hours.
- Reflow simulation through vapour phase reflow with a temperature of up to 230°C (5-10 sec on max. temperature)
- Rework simulation (ten times manual soldering) in PTH and on microvia SMD pads.
- 500 thermal cycles between -55°C and 100°C with a heating rate of 10°C/min and a dwell time of 15min at high and low temperature.
- Microsection analyses on all reworked positions.

In addition, a peel strength test in accordance with condition A of IPC-TM-650 method 2.4.8.c and an intra- and inner-layer insulation resistance and dielectric withstanding voltage test before and after thermal cycling is carried out.

Results

Thermal Analyses Test Results
The Tg of the material was measured at 258.49°C which is in line with datasheet values that list a Tg of 250-270°C using the TMA method. The measured CTE-z values were 32.36 ppm/°C below Tg and 118.1 ppm/°C above Tg. The higher CTE-z values with respect to the technical datasheet are in line with expectations when using an HDI stack with thin glass weave and high resin percentage prepregs. Summary of the results are listed in the table below. As a reference CTE-z values of the same stack in polyimide material are 61.63 ppm/°C below Tg and 164.9 ppm/°C above Tg.

Table 3. CTE, Tg test results HDI in low CTE material

	TDS value	Measured value low CTE material	Measured value PI material
CTE-z < Tg (TMA)	15-25 ppm/°C	32.36 ppm/°C	61.63 ppm/°C
CTE-z > Tg (TMA)	90-120 ppm/°C	118.1 ppm/°C	164.9 ppm/°C
Tg (TMA)	250-270 °C	258.49 °C	258.72°C

Thermal Stress Test Results
Overall, the thermal stressed microsections show a good reliability of PTHs, buried vias and microvias. No material cracks and copper cracks were observed on all sections.
For all 3 sectioned panels (S/N 1 / 3 and 4) the same non-compliances were identified with respect to ECSS-Q-ST-70-60C.

- Dielectric thickness of µ-via layers is below the minimum requirement (>60um)
- Copper thickness in PTHs is below the average minimum requirement (>25um)
- Contact dimension of µ-vias is below the minimum requirement. (>100um)

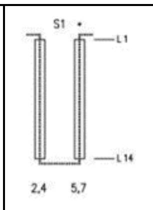
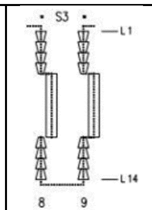
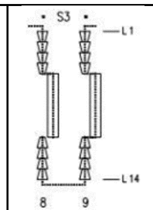
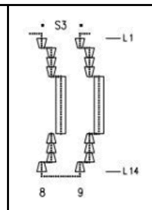
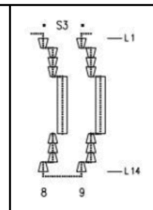
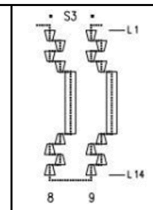
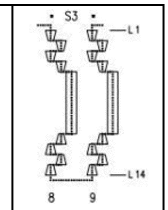
The above non-compliances with respect to ECSS-Q-ST-70-60C are all explainable through design restrictions and action taken to increase manufacturability. The dielectric thickness between the µ-via layers is measured below 60um. As the nominal thickness of the used single ply prepreg is around 80um it is logical that the dielectric thickness is around 50um after lamination. The one ply configuration was chosen specifically to increase the µ-via reliability of small diameters up to 125um. As such this is considered a non-critical non-conformance for the tested PCB technology.
The copper thickness in the PTHs was measured in average around 20um. This is below the 25um average minimum required according to ECSS-Q-ST-70-60C. This non-compliance was well expected as the copper thickness was intentionally limited to allow a feasible etching of the critical outerlayer patterns. As such the reduced PTH copper thickness is not considered a critical non-conformance. Moreover, there were no reliability issues detected on any of the sectioned PTHs before and after thermal stress.
The third non-compliance is explainable through 2 aspects: First, there is the reduced laser drill diameter of 125um which deviates from the common 150 or 175um drill diameters used in ECSS designs. Secondly, it is extremely difficult to align 4 levels of stacked microvias completely in the centre of the via in order to measure the largest contact diameter. Some of the µ-vias where a reduced contact dimension was measured are not completely in centre but are in no case related to a bad drilling quality, and do not present a reliability risk. Therefore, this is considered a non-critical non-conformance for the tested PCB technology.

IST Results

The IST testing was performed on a total of 38 IST coupons out of 6 different production panels. Four coupons were not testable and as such not submitted. of the 38 Submitted IST coupons, 36 passed the IST test without failing. One coupon was untestable as the heating circuit got damaged and one coupon failed early during preconditioning. A section analyses on this failed IST coupon could showed no anomalies and as such no root cause could be identified.

After 500 cycles there is almost no resistance increase observable on all tested coupons. The plated through holes, buried vias and microvias show an exceptional level of reliability. There is no observable difference between the different configurations and the stacked microvias can be considered as reliable as the staggered configuration. Beside this observation there are no indications that show a difference in reliability between the 150um and 125um laser drill diameters. Overall, it can be concluded that the HDI technology using low CTE material show an exceptionally high reliability during IST testing.

Table 4. IST result overview

Via Structure								
IST coupon ref.		TVX14236A	SLX14256A	SLX14257A	SLX14258A	SLX14259A	SLX14260A	SLX14261A
PTH Ø		400um	NA	NA	NA	NA	NA	NA
µ-via Ø		NA	125um	150um	125um	150um	125um	150um
Buried via Ø		NA	350um	350um	350um	350um	350um	350um
Coupons Tested		6	6	6	4	5	5	6
Coupons Passed		6	6	6	3(*)	4(**)	5	6
S1 PTH/Buried Vias 500 cycles @ 150°C	Min. Cycles	500	500	500	500	500	500	500
	Max. Cycles	500	500	500	500	500	500	500
	Avg. Cycles	500	500	500	500	500	500	500
	Min. Resistance	-0.2%	0.1%	-0.4%	0.1%	-0.2%	0.0%	-0.1%
	Max. Resistance	0.1%	0.3%	0.2%	0.4%	0.1%	0.3%	0.3%
	Avg. Resistance	0.0%	0.2%	0.0%	0.2%	0.0%	0.1%	0.1%
S3 µ-Vias + Buried vias 500 cycles @ 150°C	Min. Cycles	NA	500	500	500	500	500	500
	Max. Cycles	NA	500	500	500	500	500	500
	Avg. Cycles	NA	500	500	500	500	500	500
	Min. Resistance	NA	-0.3%	-0.2%	0.1%	-0.6%	0.0%	0.0%
	Max. Resistance	NA	0.3%	0.3%	0.3%	0.2%	0.3%	0.2%
	Avg. Resistance	NA	0.0%	0.0%	0.2%	-0.2%	0.1%	0.1%
S2 µ-Vias EXTRA 500 cycles @ 190°C	Min. Cycles	NA	500	500	500	500	500	500
	Max. Cycles	NA	500	500	500	500	500	500
	Avg. Cycles	NA	500	500	500	500	500	500
	Min. Resistance	NA	-0.1%	-0.4%	0.0%	-0.1%	0.0%	-0.2%
	Max. Resistance	NA	0.1%	0.2%	0.1%	0.2%	0.2%	0.2%
	Avg. Resistance	NA	0.0%	-0.1%	0.0%	0.0%	0.1%	0.0%

(*) 1 coupon SLX14258A was untestable due to a mechanical damage on the heating circuit.

(**)1 coupon SLX14259A failed during preconditioning. Root cause could not be identified after microsection analyses.

Assembly and life test Results

A total of seven reworked positions were sectioned and verified against ECSS-Q-ST-70-60C acceptance criteria.

A explained above, the copper thickness in the PTHs was kept low to ease the etching of the outer layer's narrow features. Surprisingly the sectioned PTHs showed no anomalies after rework and thermal cycling. All sectioned microvia positions showed an impeccable quality. There was no observed difference in reliability between 125um or 150um microvia diameters as no interface issues could be observed on any of the sections. Buried vias were also verified with no observed anomalies. Typical material related anomalies like pad lift cracks an dielectric cracks that could be induced during the excessive and harsh rework conditions were absent on all sections. Overall, the section results after assembly and life testing confirms the high level of reliability observed during IST testing. Severe rework conditions and thermal cycling did not show any fatigue of the copper structures or led to cracks in the dielectric material.

Peelstrength measured after thermal cycling was around 9 N/Cm. The intra- and inner-layer insulation resistance and dielectric withstanding voltage test before and after thermal cycling was also successful without any failures.

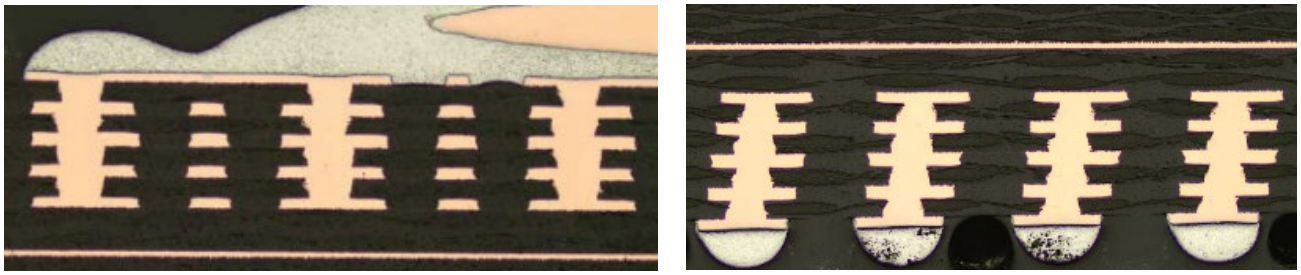


Figure 3. Cross section overview of the reworked 150um (left) and 125um (right) full stacked µ-via configuration

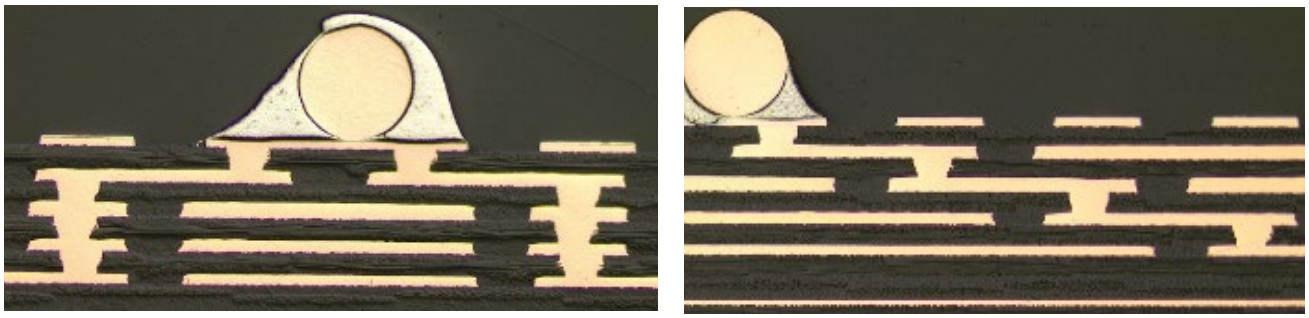


Figure 4. Cross section overview of the reworked semi-stacked (left) and full staggered (right) µ-via configuration

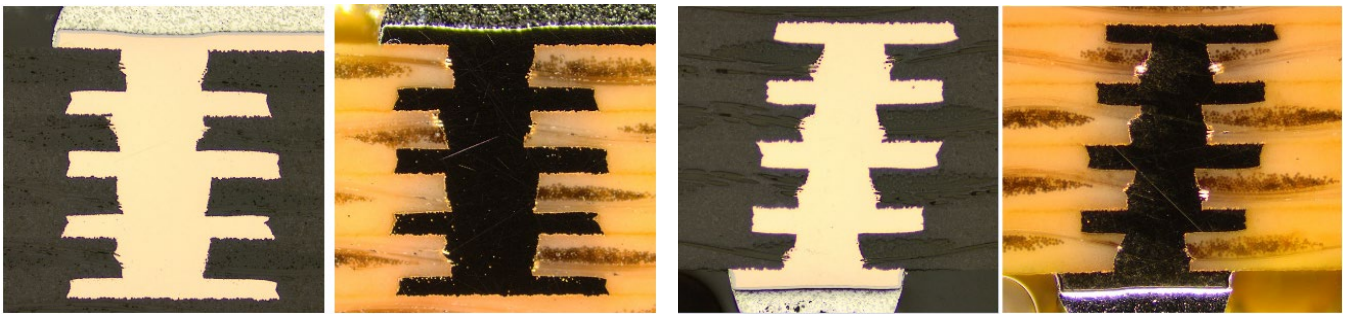


Figure 5. Cross section detail of the reworked 150um (left) and 125um (right) full stacked µ-via configuration

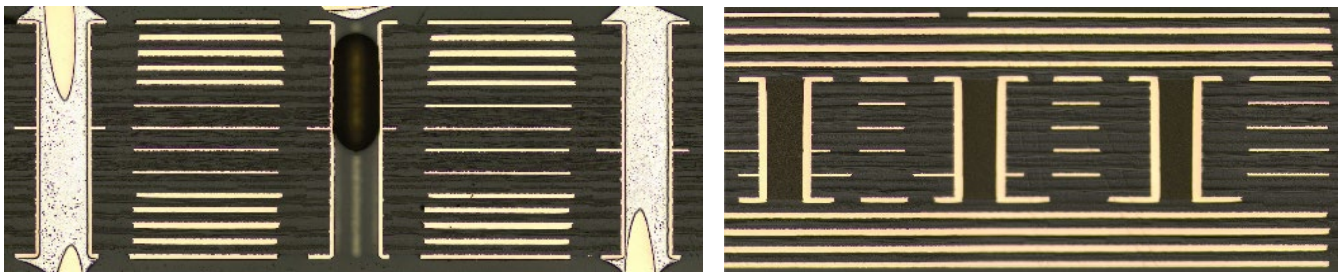


Figure 6. Cross section overview of reworked PTH (left) and buried vias (right)

Conclusions

As one of the major ECSS reliability tests for PCB technology qualification, IST results were considered critical to assess the reliability of the HDI PCB technology. Overall, we can conclude that all tested configurations were tested successfully and that no major differences were observable between the fully staggered and full stacked microvia configuration.

No defects were observed on all via configurations after thermal stress testing an assembly and lifetime testing of the PCB. Severe rework conditions and subsequent thermal cycling did not result in any detectable fatigue of the copper structures or lead to cracks in the dielectric material.

Overall, the results prove that the HDI PCB technology with a large complexity is highly robust and reliable when using low CTE material. The use of low CTE material allows the use of complex HDI configurations which is needed when using next generation components.

The results performed in this scope of the COMAP-4S project and presented in this paper form a good baseline for further technology qualifications for complex HDI technology in low CTE material. Further testing is needed in order to have a closer direct comparison between the default polyimide and low CTE material in actual space qualified HDI designs.

Acknowledgements

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