High density PCB technology for high reliability applications using Low CTE material

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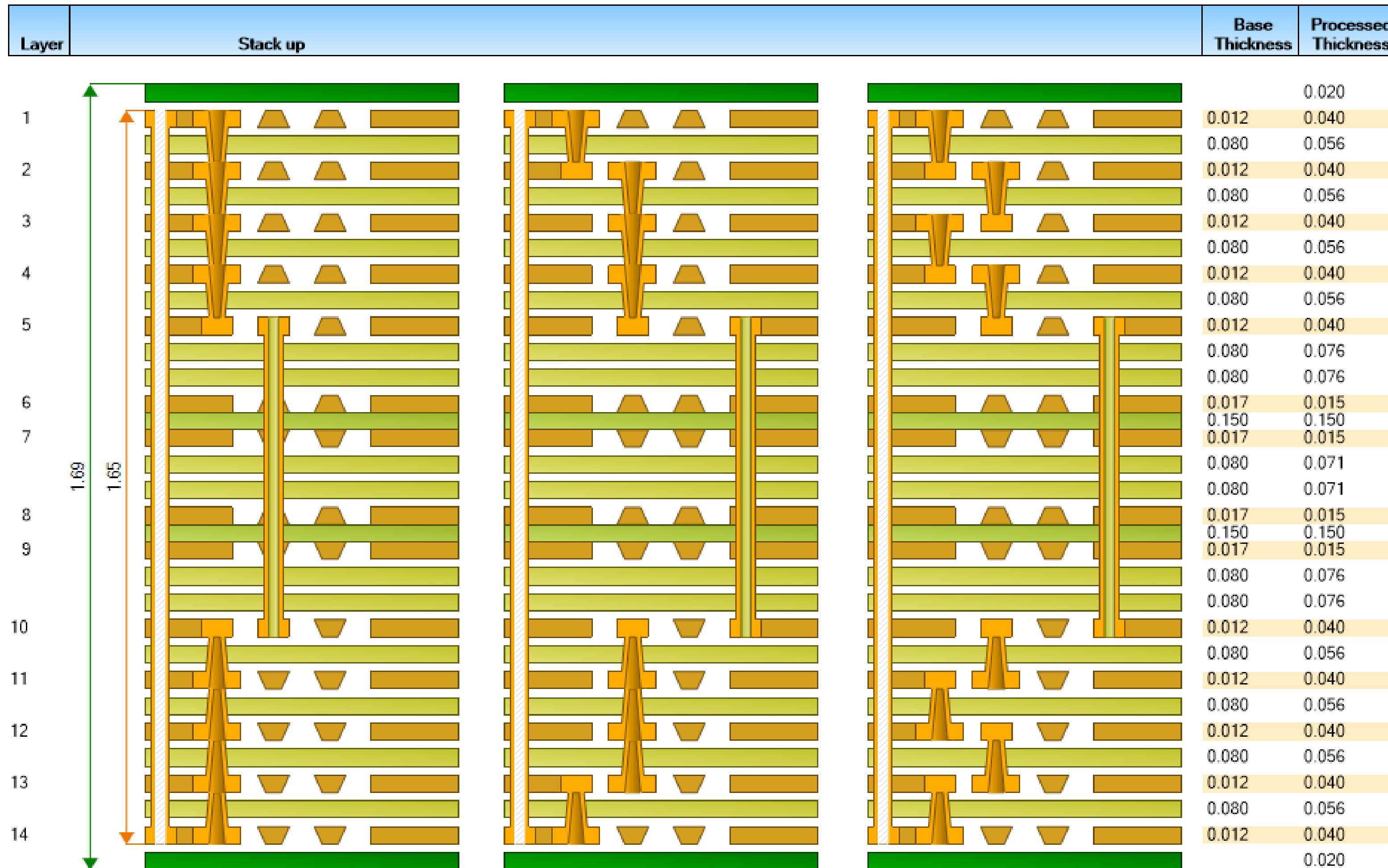
Introduction

- Today 2 levels of microvias is the most complex technology for space (ESA)
- Polyimide is the default heritage material for space
- The COMAP-4S project aims to prove reliability up to 4 levels of stacked microvias by using non-PI, ceramic-filled low-CTE material

Feature	State of the art for space	COMAP-4S
Material	PI	Low CTE
µ-via drill diameter	175um / 150um	125um
Number of µ-via levels	2	4
configuration		

Technology Overview – Test Vehicle buildup



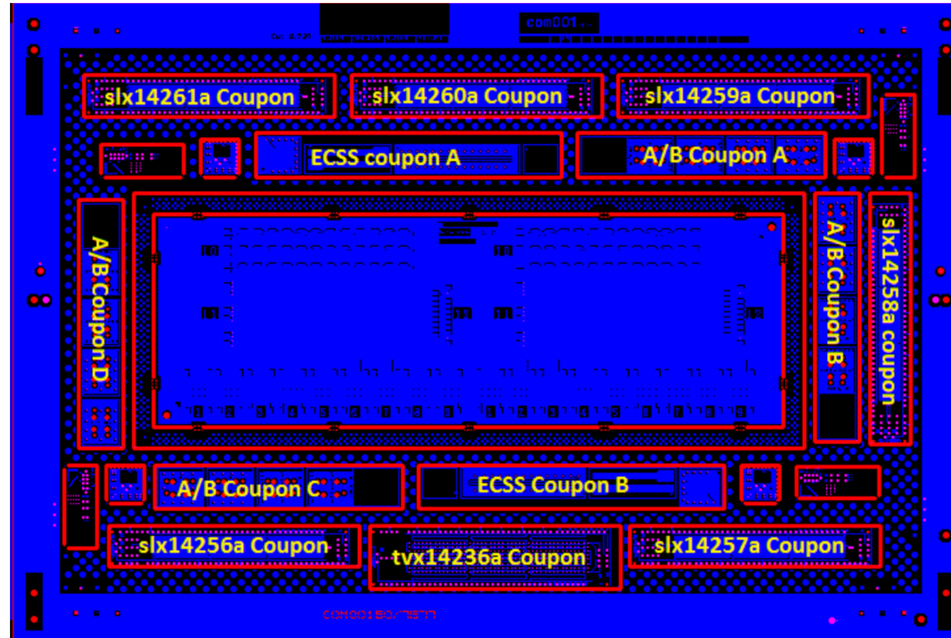
- Total of 6 different microvia patterns tested
- 3 HDI configurations ranging from all staggered to all stacked.
- 2 μ-via drill diameters (125um and 150um)
- Single ply of prepreg between microvia runs (+/- 80 um nominal)

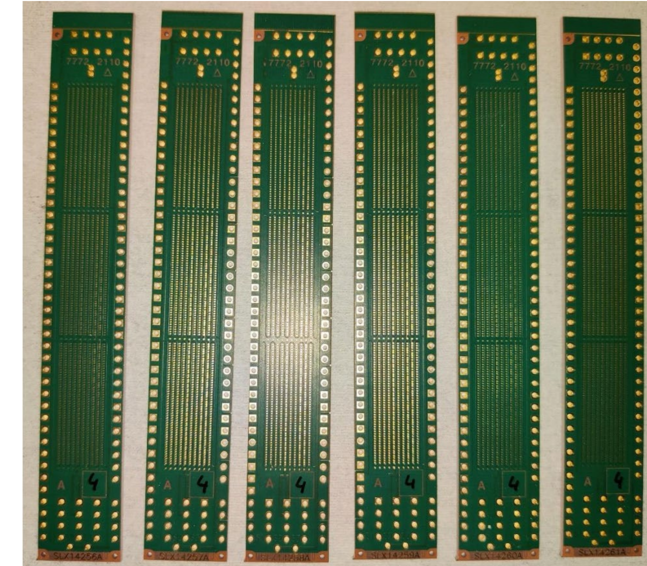
Technology Overview – Test Vehicle description

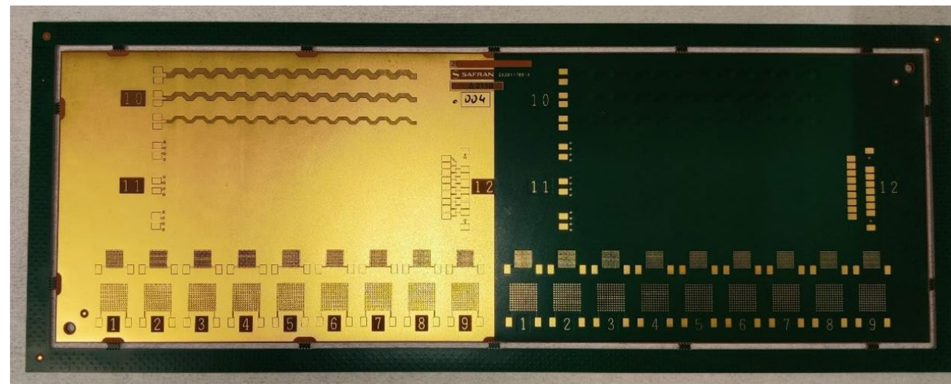
Technology Parameter	Feature value
Dielectric Material	Ceramic filled Low CTE material (Tg: >250°C, CTE-z: 15-25 ppm/°C < Tg)
Number of layers	14 layers
Number of laminations	5 laminations
number of microvia levels	4 levels
µ-via configurations	full stacked, semi stacked, full staggered
Thickness	1.7mm
conductor width and spacing plated layers (12um+plating)	50/50um , 65/65um , 75/75um
conductor width and spacing innerlayers (17um)	50/50um , 65/65um , 75/75um
Filling for core vias	Via plugging (without cap plating)
Nonfunctional pads	present on all layers
Plated through hole diameter	400um
Plated through hole pad size	700um
Buried via diameter	350um
Buried via pad size	630um
µ-via diameter	125um , 150um
µ-via pad size	300um , 350um
Surface finish and solder mask	ENEPIG with soldermask

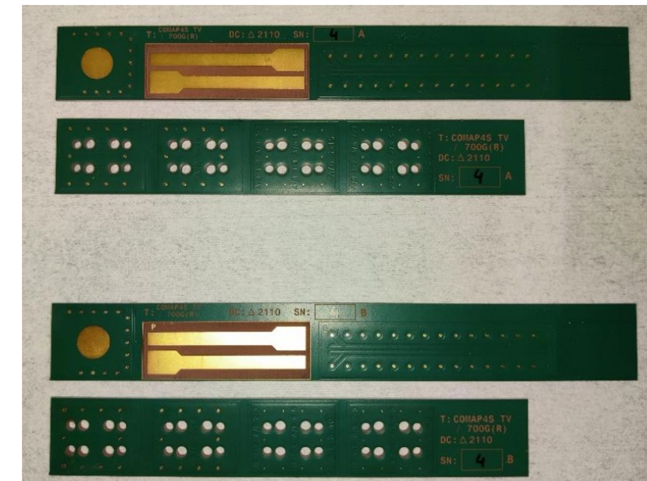
Technology Overview – Test Vehicle description

- 1x PCB
- 6x SLX IST coupon
- 1x TVX IST coupon
- 2x A/B coupon in X
- 2x A/B coupon in Y
- 2x ECSS Coupon









Test Description

- Thermal analyses test as per IPC-TM-650 2.4.24

- Thermal stress test as per condition A of IPC-TM-650 2.6.8.e
  Thermal stress test through rework as per § 9.5.4 of ECSS-Q-ST-70-60C

- Interconnection Stress Test (IST) as per IPC-TM-650 2.26A (Method A)

- Assembly and life test (Group 4) as per § 9.6.2 of ECSS-Q-ST-70-60C

Thermal analyses

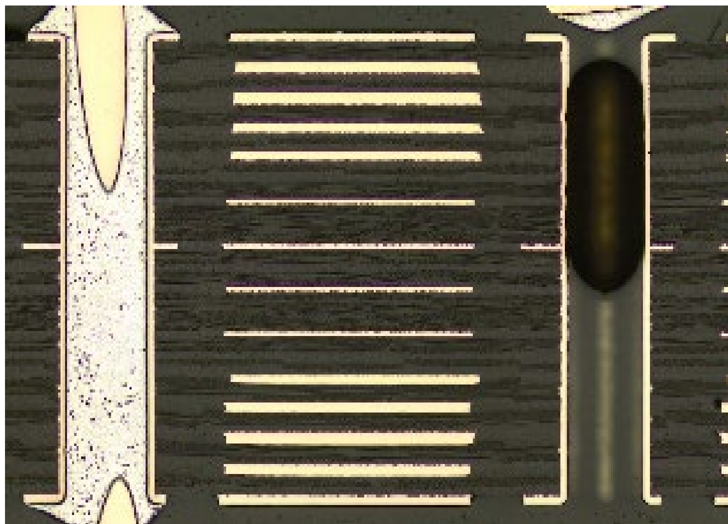
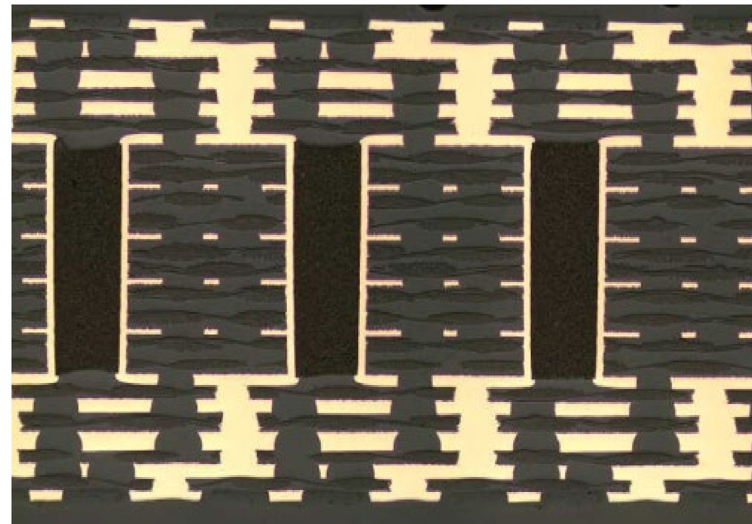
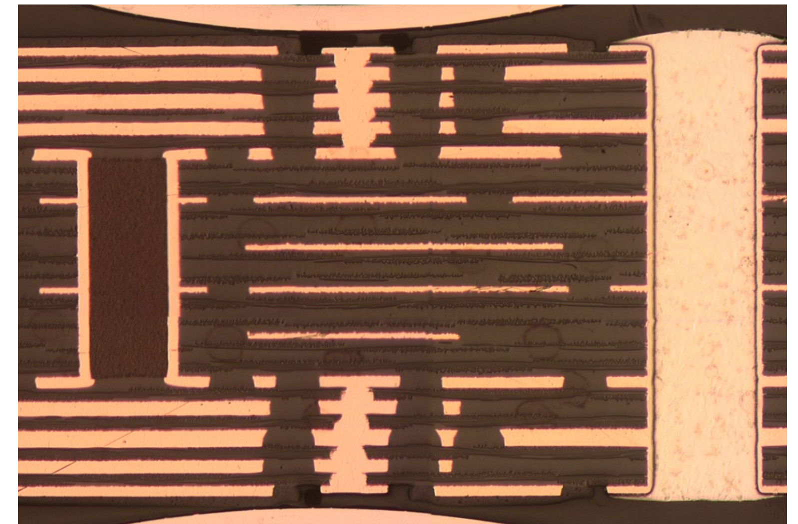
- IPC-TM-650 2.4.24
- TMA test on coupon free of copper

TMA	TDS value low CTE material	Measured value low CTE material	Measured value Polyimide material
CTE-z < Tg (ppm/°C)	15-25 ppm/°C	32.36 ppm/°C	61.63 ppm/°C
CTE-z > Tg (ppm/°C)	90-120 ppm/°C	118.1 ppm/°C	164.9 ppm/°C
Tg (°C)	250-270 °C	258.49 °C	258.72°C

- The higher CTE-z values with respect to the TDS are explained by the fact that the HDI stack contained prepregs with a thin glass weave and high resin percentage.

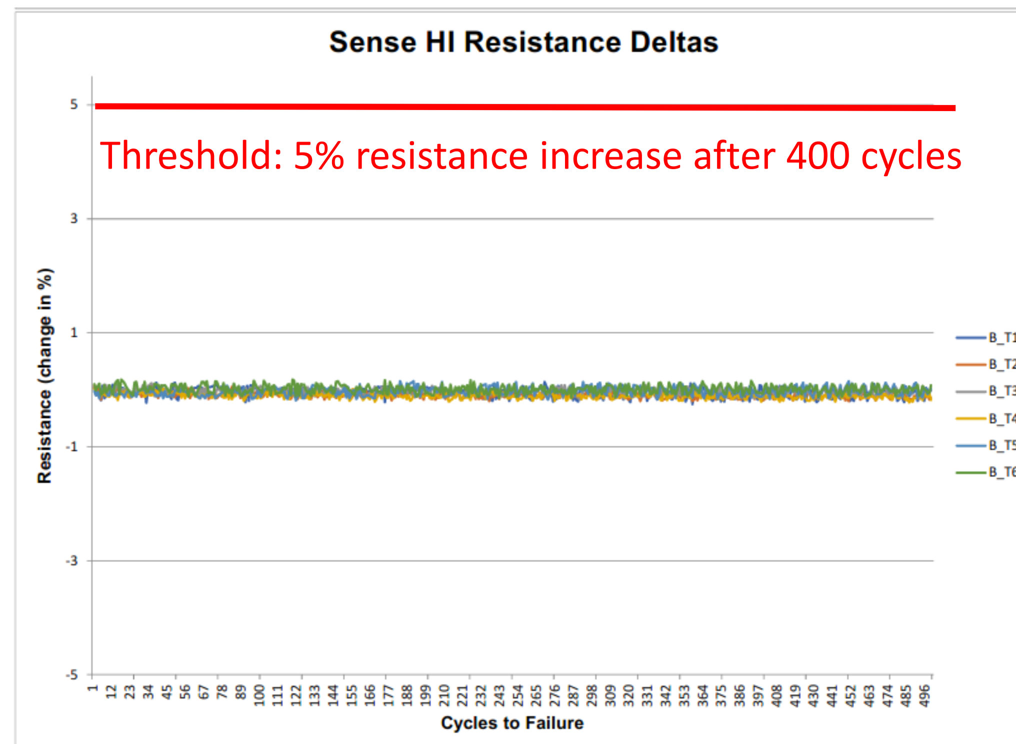
Thermal stress test

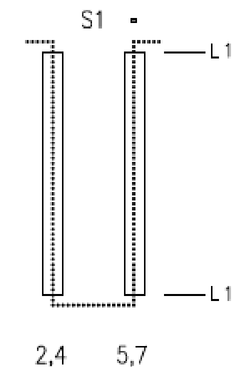
- 3x 10s solderfloat at 288°C as per IPC-TM-650 2.6.8.e
- 5 Reworks as per § 9.5.4 of ECSS-Q-ST-70-60C
- 3 observations which were as designed not compatible with ECSS-Q-ST-70-60C
  - Dielectric thickness of µ-via layers is below the minimum requirement (>60um) due to the single ply prepreg
  - Copper thickness in PTHs is below the average minimum requirement (>25um) as the surface copper on the outerlayers had to be kept as low as possible to allow fine pitch etching (50/50um TW and spacing)
  - Contact dimension of µ-vias is below the minimum requirement. (>100um) since the centering of all 4 microvia levels was challenging.

Interconnection Stress Test (IST) - PTH

- 6 TVX coupons tested
- 6 TVX coupons passed as 5% resistanc
- Maximum 0.1% resistance increase after 500 cycles at 150°C for the PTHs

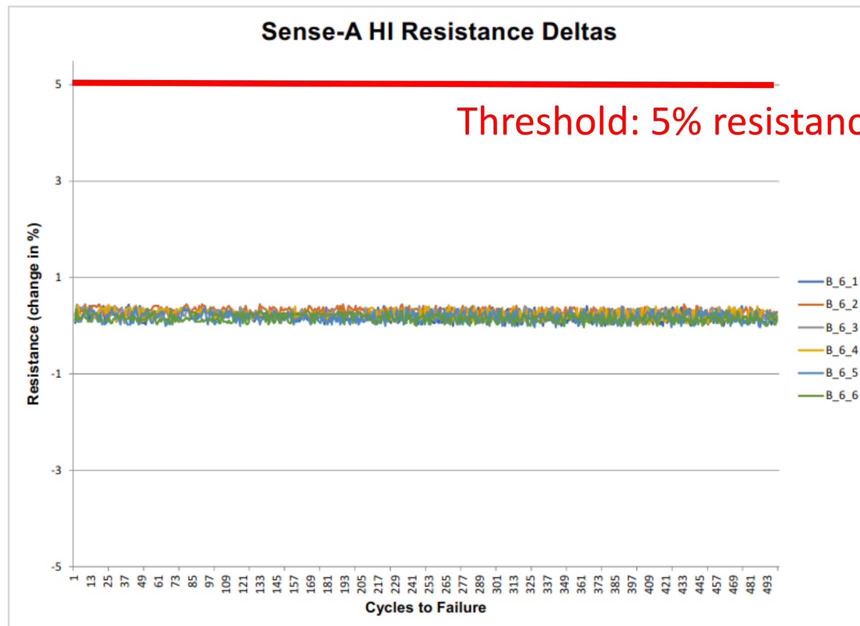




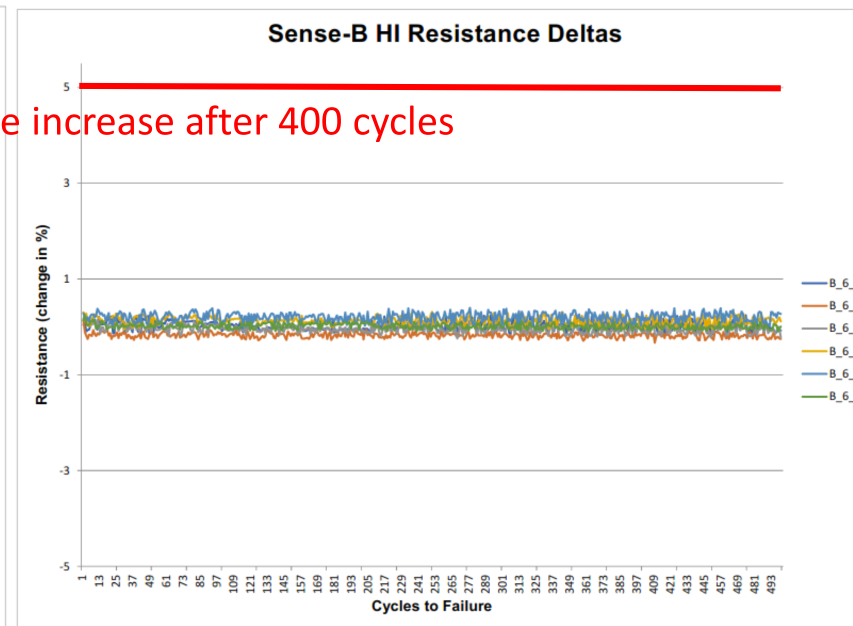
Graph of S1 for coupon TVX14236A 400um PTH

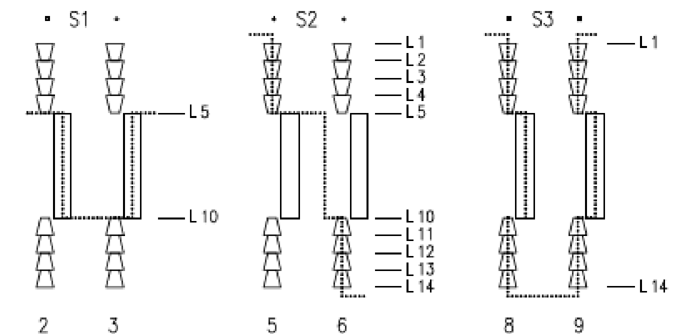
Interconnection Stress Test (IST) – Buried vias

- 32 SLX coupons with 6 different configurations tested
- 30 coupons passed
  (1 coupon had a damaged connector and 1 coupon failed without rootcause)
- Maximum 0.4% resistance increase for buried vias (S1) and maximum 0.3% resistance increase for buried and microvias (S3) after 500 cycles at 150°C



Threshold: 5% resistance increase after 400 cycles

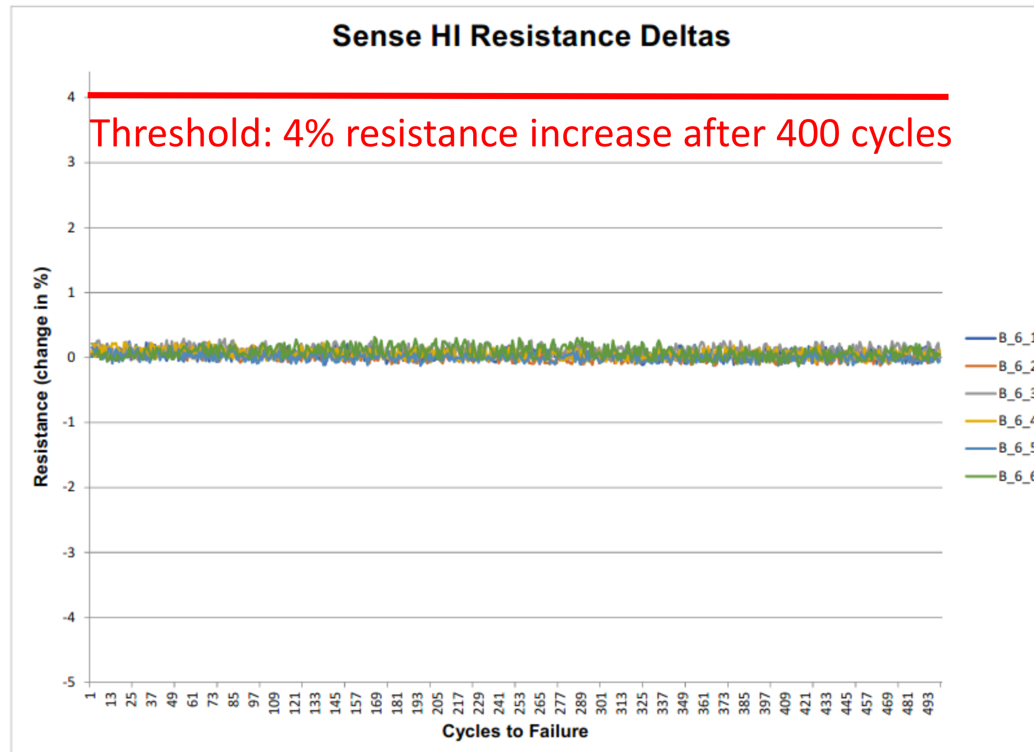


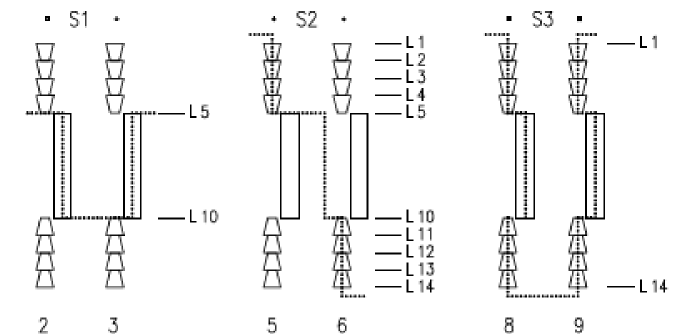


Graph of S1 and S3 for coupon SLX14256A
350um buried
4 levels of 125um µ-vias stacked

Interconnection Stress Test (IST) – µ-vias

- 32 SLX coupons with 6 different configurations tested
- 30 coupons passed
  (1 coupon had a damaged connector and 1 coupon failed without rootcause)
- Maximum 0.2% resistance increase after an additional 500 cycles at 190°C for the microvias (S2)





Graph of S2 for coupon SLX14256A
350um buried
4 levels of 125um µ-vias stacked

Interconnection Stress Test (IST)

- 38 IST coupons tested
- 6 preconditioning cycles at 230°C
- 500 cycles for PTH and Buried vias at 150°C
- 500 cycles for µ-vias at 190°C

- There is no observable difference between the different configurations and the stacked microvias can be considered as reliable as the staggered configuration.
- No observed difference in reliability between the 150um and 125um laser drill diameters.
- Overall, it can be concluded that the HDI technology using low CTE material show an exceptionally high reliability during IST testing

Assembly and life test (Group 4)

- Peelstrength after TC in line with expectations and sufficient for reliability.

N	N/mm	N/cm
2.72	0.91	9.07
2.60	0.87	8.67
2.52	0.84	8.40
2.54	0.85	8.47

- Successful insulation resistance testing before and after TC
  (Insulation resistances well above the threshold limits when applying 250V DC)
  - intralayer insulation resistance as received >10GΩ
  - Intralayer insulation resistance after TC >1GΩ
  - interlayer insulation resistance as received >100GΩ
  - interlayer insulation resistance as received >10GΩ

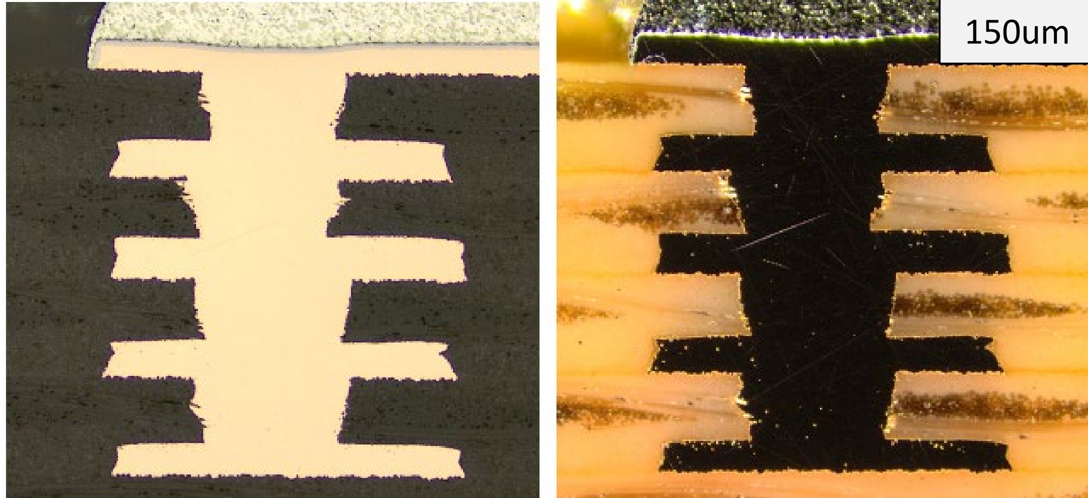
- Successful Dielectric withstanding voltage before and after TC
  (No sudden voltage drop when applying 1000V DC for 30S)

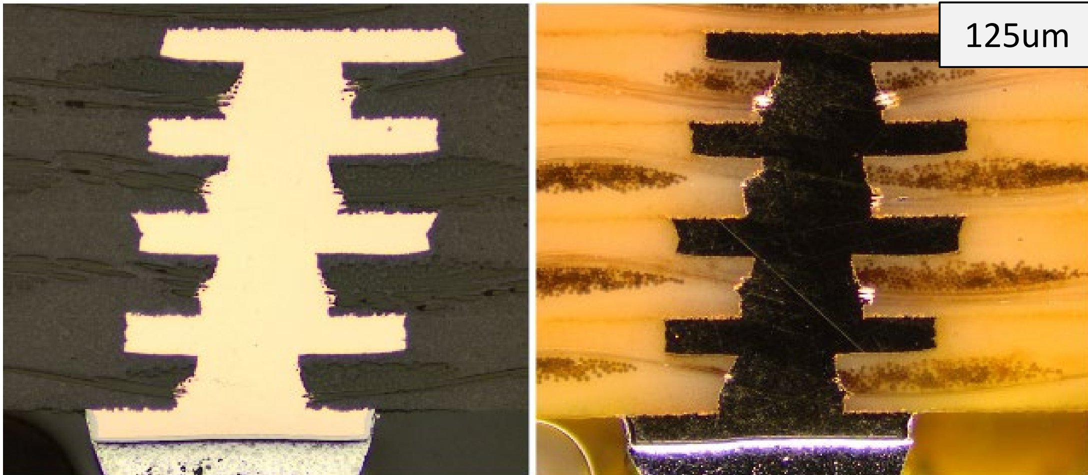
Assembly and life test (Group 4)

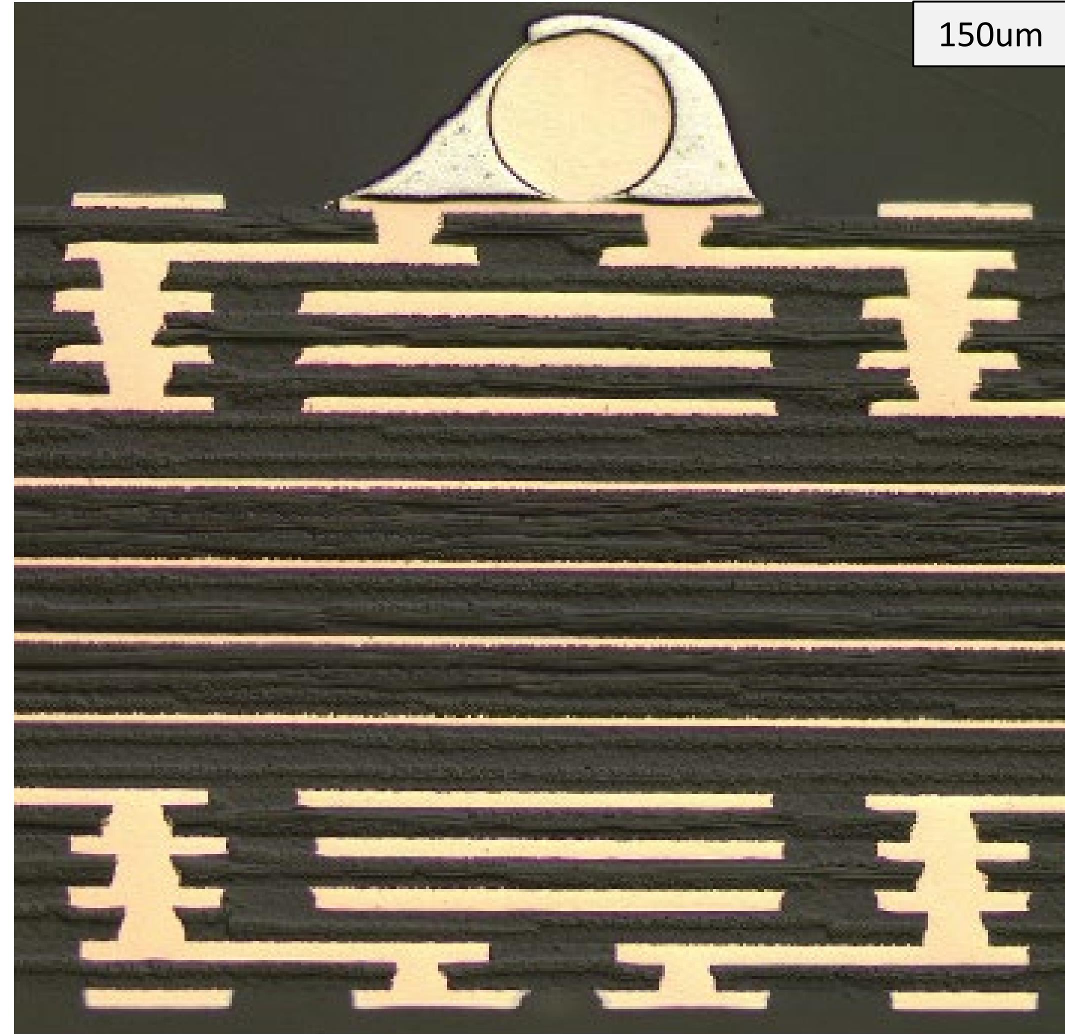
- Assembly and life test (Group 4) as per § 9.6.2 of ECSS-Q-ST-70-60C
  - Pre-conditioning/ baking of the PCB and test coupons at 120°C for 8 hours.
  - Reflow simulation through vapour phase reflow with a temperature of up to 230°C (5-10 sec on max. temperature)
  - Rework simulation (ten times manual soldering) in PTH and on microvia SMD pads.
  - 500 thermal cycles between -55°C and 100°C with a heating rate of 10°C/min and a dwell time of 15min at high and low temperature.
  - Microsection analyses on all reworked positions.

- Very good microvia quality for both 125um and 150um diameter
- No demarcation or separation visible between landing layer and µ-via
- Fully stacked condition proven as reliable as all staggered
- No copper cracks observed on PTH and Buried vias
- No dielectric cracks observed around PTH and Buried vias
- Thin copper (around 15um) in PTH still proven reliable

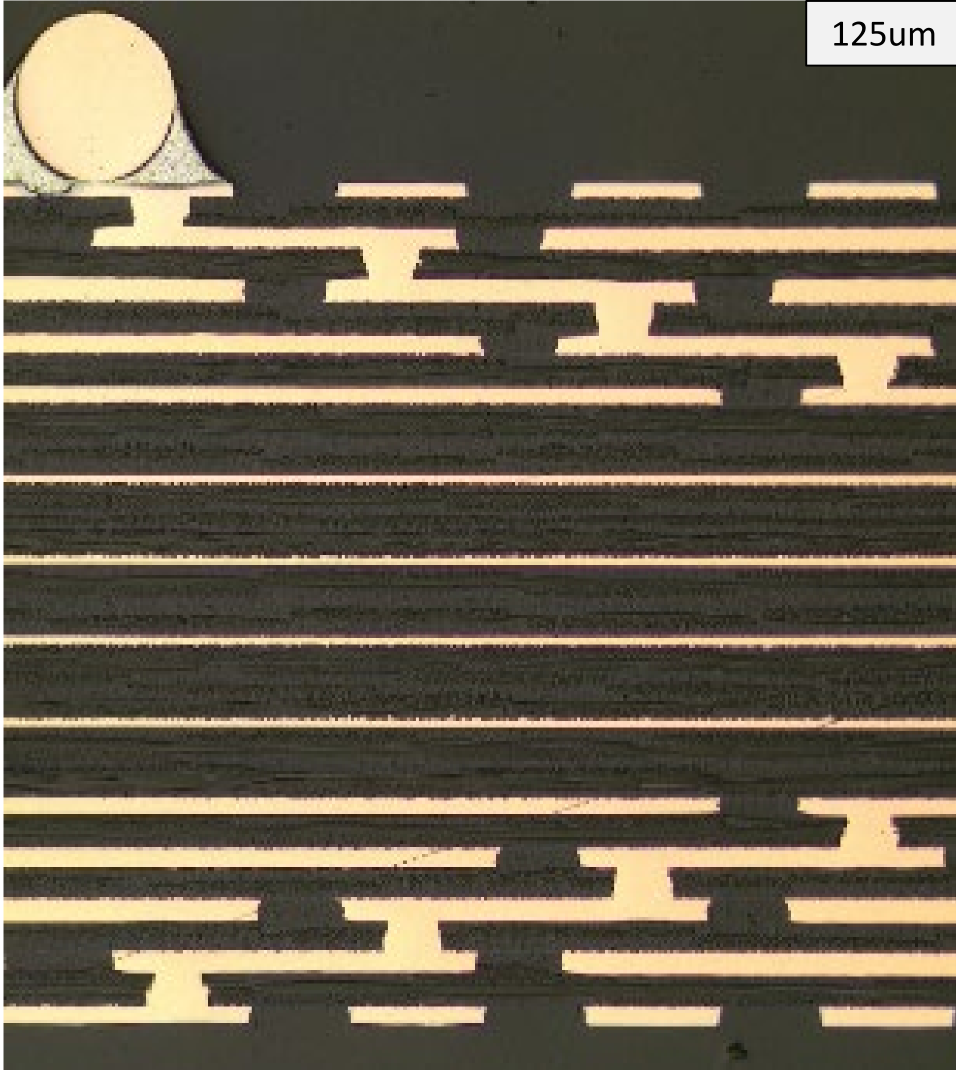
Assembly and life test (Group 4)

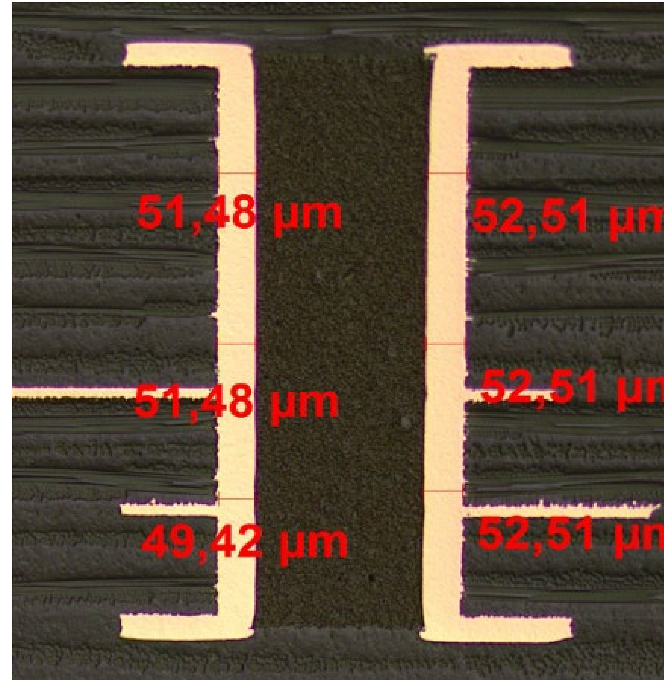


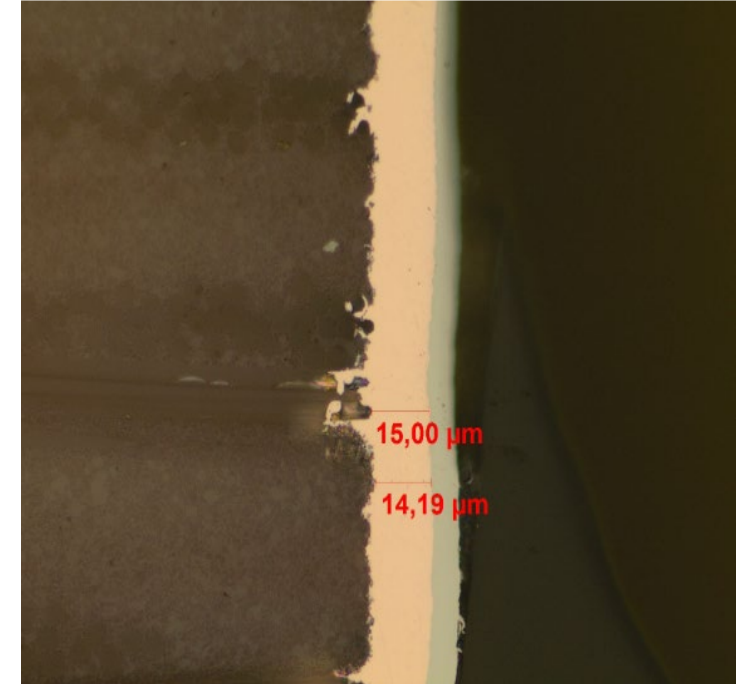


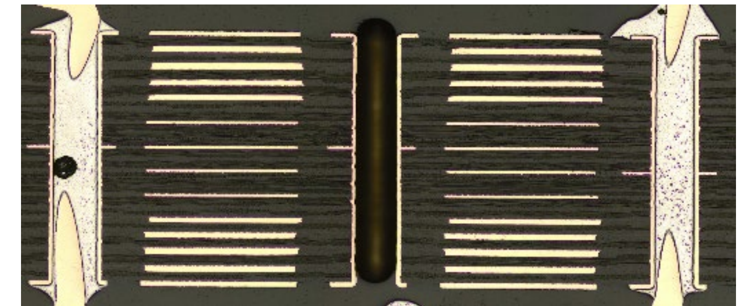


Assembly and life test (Group 4)



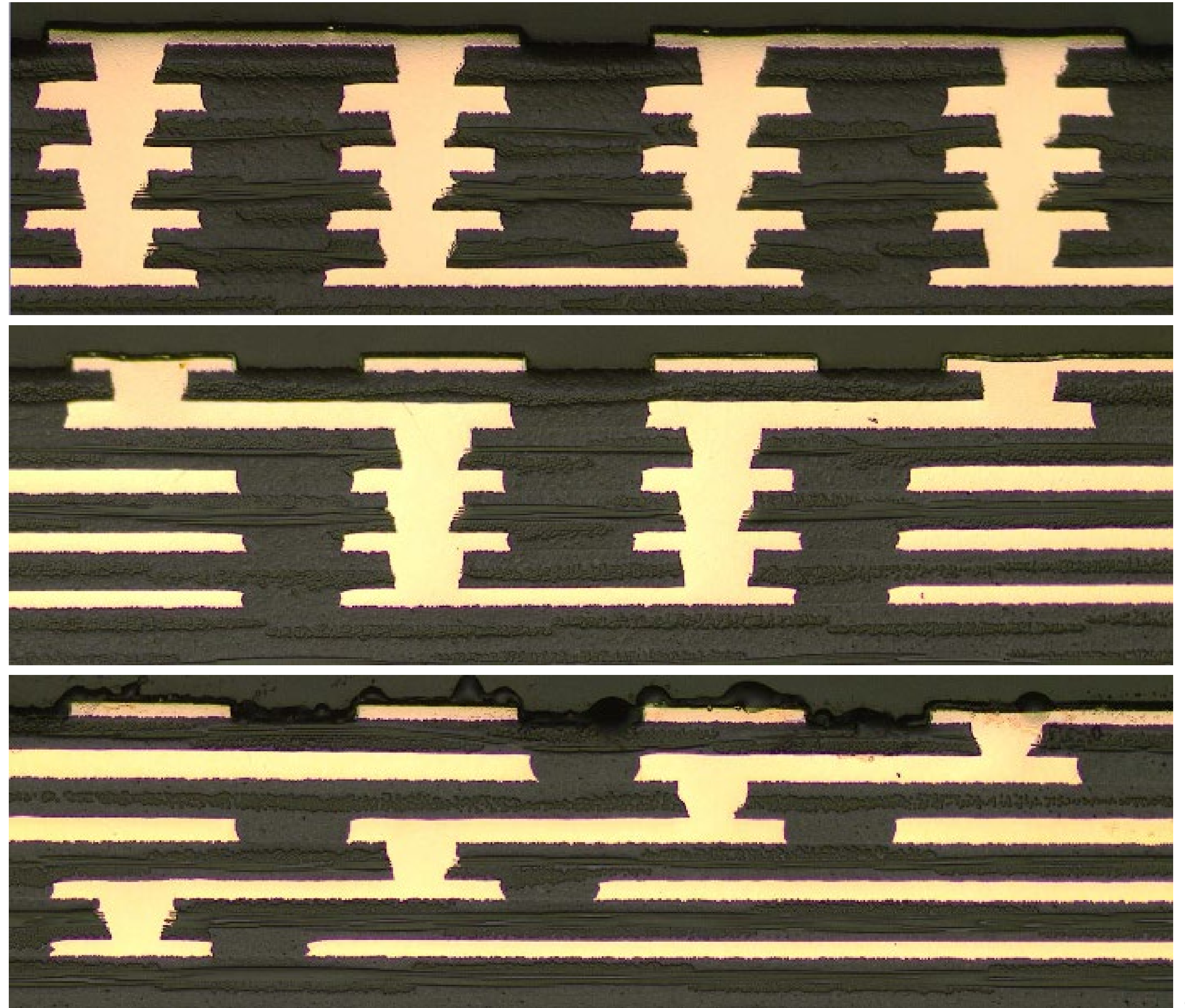






Additional thermal cycling testing

- To further demonstrate the high reliability an additional thermal cycling test was carried out
- The minimum and maximum temperatures was set at -55°C and 125°C with a dwell time of 15 minutes
- Sections were taken after 500 and 1000 thermal shock cycles on all configurations
- Not a single anomaly on all via configurations after 500 and even 1000 cycles



Comparison with PI Test vehicle

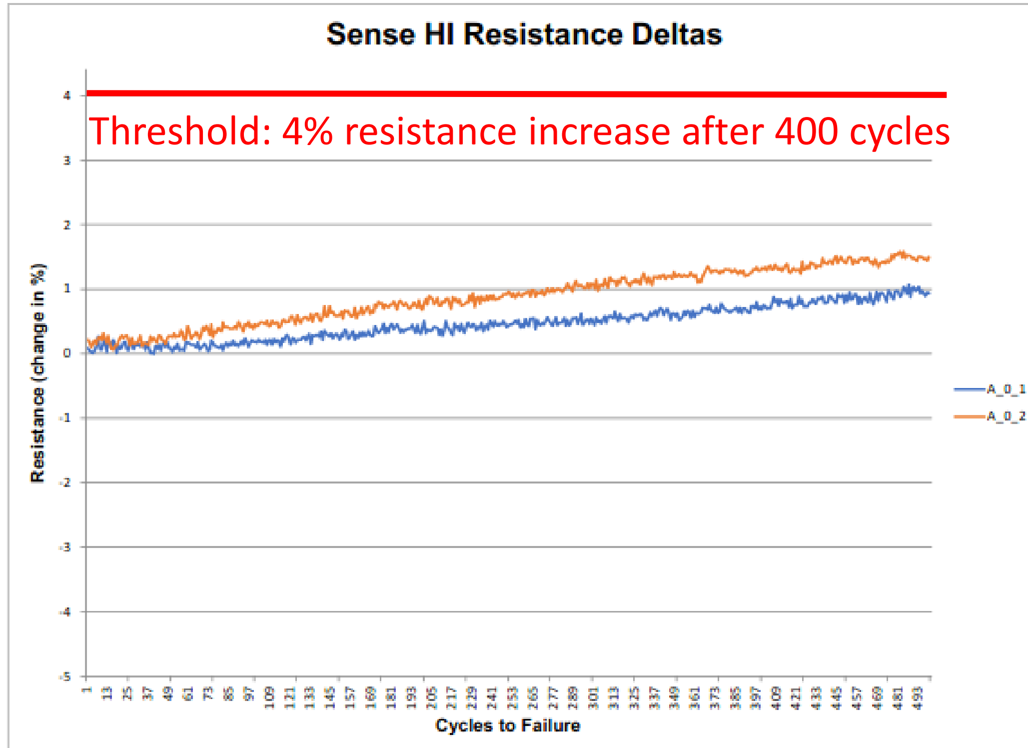
- A reference batch with the same design and µ-via configurations was manufactured to have a direct comparison between the PI and Low-CTE material.
- Only IST testing was performed to asses the reliability of the PI build.
- 2 tested TVX coupons showed a good reliability of the PTHs with a maximum resistance increase of 0.4% after 500 cycles at 170°C
- All tested pairs of coupons of the stacked and semi stacked configurations failed before the microvia cycling
- The 2 SLX14260A coupons with a fully staggered microvia configuration did pass both buried via and microvia cycling. A resistance increase of 1.5% was observed after 500 cycles at 210°C

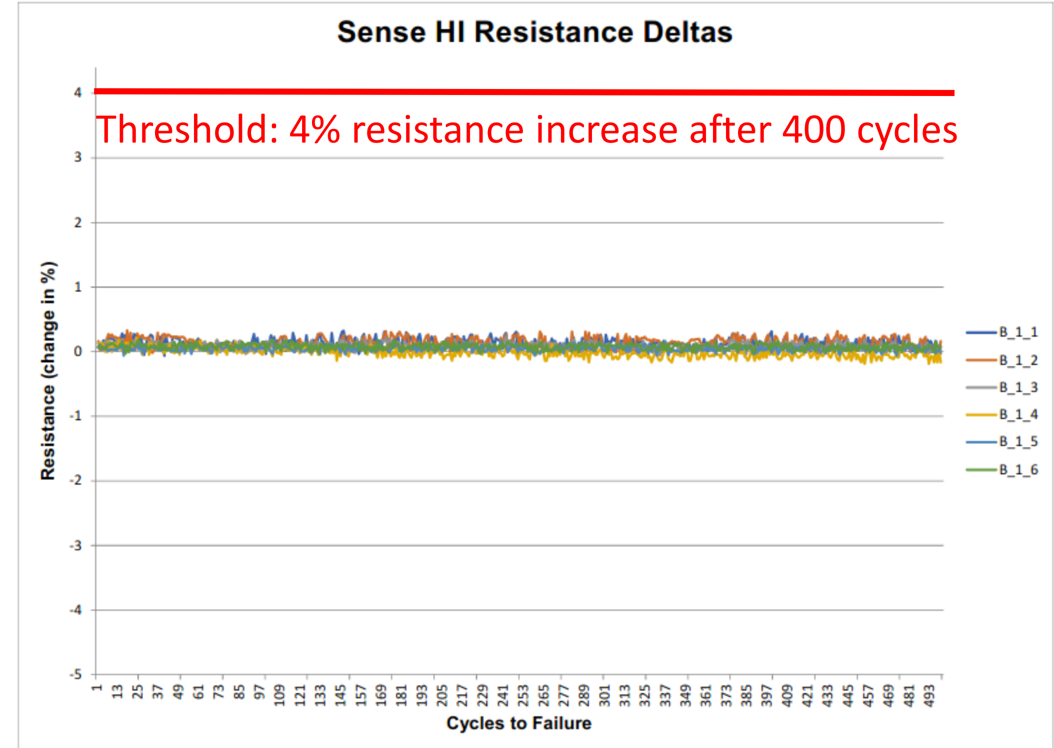
- Since all stacked configurations failed the LOW-CTE material has proven much more reliable for this complex HDI configuration

Comparison with PI Test vehicle

PI Staggered μ-via configuration

LOW-CTE Staggered μ-via configuration





Conclusion and Future work

- Reconciling the use of multiple microvia levels with the reliability requirements for space is challenging when using heritage dielectric materials (PI).
- Current test results prove that HDI PCB technology with a large complexity is highly robust and reliable when using low CTE material.

- The results performed in this scope of the COMAP-4S project form a good baseline for further technology qualifications for complex HDI technology in low CTE material.
- The next step would be to manufacturing a reference HDI design qualified for space applications in the low CTE material in order to get a direct comparison with the currently used Polyimide materials.

Questions?